

WHAT IS CLAIMED IS:

5 1. A signal processing system having a variable frequency input clock comprising:

 phase detection means for generating an error signal representing phase difference between said variable frequency input clock and a first clock,

10 filtering means coupled to said phase detection means for filtering said error signal,

 a numerically controlled oscillator, responsive to said filtered error signal and a sample clock for providing said first clock; and

15 buffering means for receiving an input signal at the variable frequency input clock and responsive to said first clock, outputting a data signal at said first clock.

20 2. The signal processing system of claim 1 further comprising interpolation means coupled to the buffer means, wherein said interpolation means is responsive to a phase offset signal representing an offset in phase between the sample clock and the first clock.

25 3. The signal processing system of claim 2 further comprising a modulation means for modulating the interpolated signal with a trigonometric signal having a carrier frequency to form a modulated signal.

30 4. The signal processing system of claim 3 further comprising a digital to analog converter for converting said modulated signal to an analog signal.

35 5. A signal processing system comprising:
 means for providing a first clock at a first clock

frequency as a function of a sample clock having a sample clock frequency and a variable frequency input clock;

5 buffering means for receiving an input signal at the variable frequency input clock and, responsive to said first clock, outputting a data signal at said first clock frequency; and

10 interpolation means, responsive to a phase offset signal, representing an offset in phase between the sample clock and the first clock, coupled to the output of the buffering means for providing an interpolated signal at the sample clock frequency.

15 6. The signal processing system of claim 5 wherein the interpolation means interpolates the data signal by a non-integer value.

20 7. The signal processing system of claim 5 wherein the interpolation means interpolates the data signal by an integer value.

25 8. The signal processing system of claim 5 further comprising modulation means for modulating the interpolated signal with a trigonometric signal having a carrier frequency to form a modulated signal.

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